Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 2. This sheet, replaces the original sheet including Fig. 2. In Figure 2, previously omitted text "(Prior Art)" has been added.

Attachment: Replacement Sheet Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Paragraphs 0018 – 0023 have been amended to more correctly describe the claimed invention and correct typographical, grammatical and antecedent basis errors.

Figure 2 was amended to add the text "(Prior Art)" as requested by the Examiner.

Claims 1-13 and 15-17 remain in this application. Claims 1- 8, 10-12 and 15 have been amended to more clearly describe the claimed and invention and correct typographical, grammatical and antecedent basis errors. Claim 14 was cancelled.

Claims 1, 4 and 12-15 were rejected under 35 USC 103(a) as being unpatentable over Starke et al. (US Patent No. 6,643,763) in view of Check et al. (US Patent No. 6,990,556). Claim 1 includes the limitations, a system bus for connecting a first transmission channel and a second transmission channel with a command processor and adjusting a transmitting direction of the system bus according to a transmitting direction of the second transmission channel. This structure is disclosed in the application at paragraph 0018 with reference to Fig. 1B (reproduced below). The bus 140 couples the first channel 120 and the second channel 130 to the command processor which has been added to Fig. 1B for clarity.

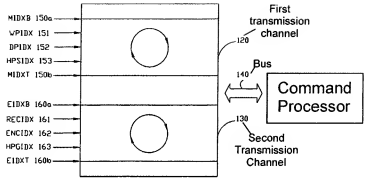
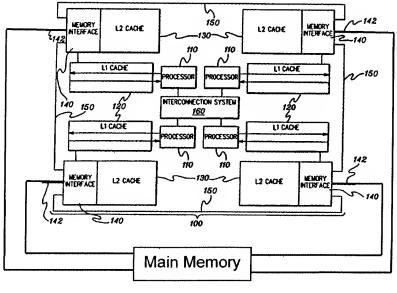


FIG.1B

In contrast to the claimed structure, the Examiner argues that Starke discloses methods for transferring data between a first processing engine 110 and a second processing engine 110 using a register pipe 150, wherein data is transferred between the first and second processing engines 110 without passing through a main memory of the multiprocessor computer system. (Office Action, page 4.) (Starke, Col. 5, lines 13-15.) Fig. 1 of Starke has been modified to correspond with this description and is illustrated below:



The applicant respectfully submits that Stark discloses four individual processor modules that each includes a processor 110, L1 cache 120, memory interface 140 and L2 cache 130. The processor modules communicate with each other by four bi-directional buses 150 as well as the interconnection system 160. The memory interfaces 140 are also coupled to a main memory via buses 142. (Starke, Col. 5, lines 13-15.) As discussed, the buses 150 transmit data directly to the processor modules to avoid transmitting the data through the main memory and buses 142. Since buses 142, 150 are used independently, Starke teaches away from using the bi-directional buses 150 to couple the processors to transmission channels 142. For these reasons, the applicant respectfully submits that Starke does not disclose the limitation of a bus connecting the first and second transmission channels to a command processor or adjusting a transmitting direction of the system bus according to a transmitting direction of the second transmitting channel.

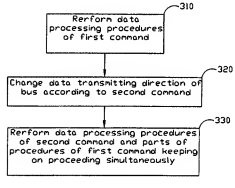
The Examiner also argues that Check discloses a cache storage which reads data from a single double word in the cache storage and simultaneously provides the doubleword to the first pipe and the second pipe in response to the same doubleword signal. (Office Action, page 4) The applicant submits that the system disclosed by Check performs multi-step sequential processing that is illustrated in Fig. 1 reproduced below. The processing includes the steps: instruction decode 100, address generation 101, cache directory and interleave read 102, data validation and return 103, execution 104, and put away 105. "Embodiments of the invention allow for multiple (e.g., two) instructions to execute together during the execution cycle 104 which return data together during the cache return cycle 103 for which the data for both instructions are the same doubleword in cache." (Check, Col. 2, lines 53-60, Fig. 1.) The

applicant respectfully submits that Check discloses the simultaneous processing of two instructions and the simultaneous transmitting of the data during the cache return cycle 103. Thus, the processor receives the two instructions from the bus, performs the instructions and then transmits the return data back through the bus.

#100	#101	#102	#103	#104	#105
DECODE	ADDRESS GENERAT-ION	CACHE READ	CACHE HIT & DATE RETURN	EXECUTION	PUT-AWAY

FIG. 1

Claim 1 was amended to more clearly describe the limitation that the data processing procedures of the first transmission channel occur during the adjusting of the transmitting direction of the system bus. In contrast to Check, the data processing of the first command occurs while the data transmitting direction of the bus is changed. This limitation is disclosed in the application at paragraphs 0019 – 0020 and Figs. 3 and 4. Fig. 3 has been reproduced below.



For the reasons discussed above, the applicant submits that the prior art cited by the Examiner does not disclose all claim limitations and that claim 1 is not invalid under 35 USC 103(a) over Starke in view of Check.

Claim 4 as amended includes the limitations "determining a data transmission channel of said data transmission channel module according to a command issued by a command processor." This limitation was not discussed in the Office Action. Claim 4 as amended also includes the limitation, "performing parts of a processing procedure of a first transmission channel of said data transmission channel module during a time period when a second transmission channel of said data transmission channel module is using a common transmitting path." As discussed above, the applicant submits that Check discloses that transmission of the data and data processing occur simultaneously. Thus, processing of a first transmission channel does not occur when the second transmission channel is using the common transmitting path. For these reasons, the applicant submits that all limitation of claim 4 are not disclosed by Starke or Check and claim 4 is not invalid under 35 USC 103(a) over Starke in view of Check.

Claim 12 has been amended to add the limitations of claim 14. Thus, claim 12 is effectively claim 14 rewritten in independent form. As discussed in the Office Action, the Examiner acknowledged that claim 14 is directed towards patentable subject matter. For this reason, the applicant submits that claim 12 as amended is allowable and not invalid under 35 USC 103(a) over Starke in view of Check. Claims 13 and 15 depend from claim 12 and for these same reasons, the applicant submits that claims 13 and 15 are not invalid under 35 USC 103(a) over Starke in view of Check.

On page 5 of the Office Action, the Examiner has acknowledged that claims 2, 3, 5-11, 16 and 17 are directed towards patentable subject matter. The applicant thanks the Examiner for

this recognition. However, for the reasons stated above, claims 2, 3, 5-11, 16 and 17 have not been rewritten in independent form.

Applicant requests that the above described amendments be made part of the official record in the present application and respectfully requests that a timely Notice of Allowance be issued in this case. The Commissioner is hereby authorized to charge any underpayment of fees associated with this communication or credit any overpayment to Deposit Account No. 04-0822.

Respectfully submitted,

DERGOSITS & NOAH LLP

Dated: January 7, 2008

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